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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,838	04/13/2004	Tomohiro Ueda	251805US6	3228

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EXAMINER	
SURYAWANSHI, SURESH	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 08/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,838	UEDA, TOMOHIRO	
	Examiner	Art Unit	
	Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 are presented for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. Independent claim 1 recites the limitation of " . . . each of the first circuit and the second circuit having a normal operation state and a standby state, . . ." But the applicant expressly discloses that the standby controlling circuit (the first circuit) is a block to which power is always supplied. Please see page 7 and lines 13-15 of the specification. Therefore, the first circuit does not have two mode of operation (a normal operation state and a standby state) as it remains always on.

5. Similarly, independent claim 8 recites the limitation of " . . . each of the first circuit and the second circuit has a normal operation state and a standby state, . . ." But the applicant expressly discloses that the standby controlling circuit (the first circuit) is a block to which power is always supplied. Please see page 7 and lines 13-15 of the specification. Therefore, the first circuit does not have two mode of operation (a normal operation state and a standby state) as it remains always on.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ooishi (US Patent 6,914,845) in view of Lutkemeyer (US Patent 6,879,196).

8. As per claim 1, Ooishi discloses

power controlling means for supplying power to the first circuit and the second circuit in the normal operation state and for supplying power to only the first circuit in the standby state [Fig. 1; col. 4, lines 9-34; to reduce power consumption, power control unit supplies power to

only those logic circuits that are needed for the operation, and sets a circuit block which is not need for the operation to a standby state by shutting off the power]; and

controlling means for copying contents that are set to the first register to the second register when the state changes from the standby state to the normal operation state [Fig. 1; col. 4, lines 9-34; restoring the data saved in memory unit in the circuit block].

Ooishi does not disclose about clock controlling means for controlling generation of a first clock and a second clock. However, Lutkemeyer clearly discloses that it is well know in the art and typically implemented in an integrated circuit where multiple supply voltages are used to reduce the power dissipation of the integrated circuit [fig. 1; col. 3, lines 37-54]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to a number of circuits in an integrated circuit and trying to reduce the power dissipation of the integrated circuit by selectively shutting off the power to a circuit that is not needed for the operation.

9. As per claim 8, Ooishi discloses

controlling power supplied to the first circuit and the second circuit so as to supply the power to the first circuit and the second circuit in the normal operation state and the power to only the first circuit in the standby state [Fig. 1; col. 4, lines 9-34; to reduce power consumption,

power control unit supplies power to only those logic circuits that are needed for the operation, and sets a circuit block which is not need for the operation to a standby state by shutting off the power]; and

copying contents that are set in the first register that is disposed in the first circuit and operated with the first clock to a second register that is disposed in the first circuit and operated with the second clock when the state changes from the standby state to the normal operation state [Fig. 1; col. 4, lines 9-34; restoring the data saved in memory unit in the circuit block].

Ooishi does not disclose about clock controlling means for controlling generation of a first clock and a second clock. However, Lutkemeyer clearly discloses that it is well know in the art and typically implemented in an integrated circuit where multiple supply voltages are used to reduce the power dissipation of the integrated circuit [fig. 1; col. 3, lines 37-54]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to a number of circuits in an integrated circuit and trying to reduce the power dissipation of the integrated circuit by selectively shutting off the power to a circuit that is not needed for the operation.

10. As per claim 2, Lutkemeyer discloses that the frequency of the first clock is lower than the frequency of the second clock [col. 1, lines 42-50].

11. As per claim 3, Ooishi discloses that data is set to the second register not through the first region in the normal operation state [Fig. 1; col. 4, lines 16-23].

12. As per claim 4, Ooishi discloses that the contents of the second register are read by a CPU disposed in the second circuit [Fig. 1; inherent to the system].

13. As per claim 5, Ooishi discloses that information of an event is set from an input device disposed outside the semiconductor integrated circuit to the first register [Fig. 1; col. 3, lines 56-57; terminal EXIO].

14. As per claim 6, Ooishi discloses that the power is supplied from a battery [Fig. 1; inherent to the system as in case of a laptop or handheld computer].

15. As per claim 7, Ooishi discloses the contents that have been set to the first register are copied to the second register in parallel in one period of the first clock [Fig. 1; col. 4, lines 9-34; restoring the data saved in memory unit in the circuit block].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

sks
July 27, 2006

THOMAS LEE
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